

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE Docket No.: CYPR-CD00055
Thereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit. signature of the Person Name of Person 05/08/03 ANTHONY CHOU Making the Deposit: Deposit: Making the Deposit: Inventor(s): James Daniel Merchant, Gordon Carsksdon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak and Andrew Wright Serial No.: 09/684,160 Group Art Unit: 2172 Filed: 10/04/00 Examiner: Hamilton, M. G. Confirmation No: Title: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF CONFIGURATION BITS FROM A SCHEMATIC HIERARCHY Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 MAY 1 3 2003 Technology Center 2100 Sir: TRANSMITTAL OF FORMAL DRAWINGS In response to Drawing Informalities attached please find: the formal drawings for this application X | (a) Number of Sheets X Each sheet of drawing indicates the identifying indicia suggested in § 1.84(c) on the reverse side of the drawing a copy of the NOTICE OF INFORMAL DRAWINGS Please direct all correspondence concerning the above-identified application to the following address: WAGNER, MURABITO & HAO LLP Two North Market Street, Third Floor San Jose, California 95113 (408) 938-9060 Respectfully submitted,

5/8/03 Date:

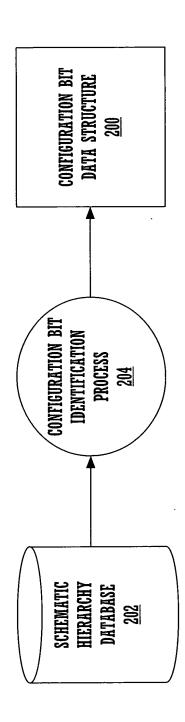
Ronald M. Pomerenke Reg. No. 43,009

Nayak, Andrew Wright
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INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup

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						1	
		Instance Path <u>226</u>	"top" "memory" "inst3" "mc<0>" "inst18" "c<0>"	"top" "memory" "inst3" "mc<0>" "inst42" "c<0>"		Instance Path 226	"top" "memory" "inst5" "mc<0>" "inst8" "c<0>"
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		wordLine <u>220</u>	<()>/M	<()>/M	 "libraryName1/Cellname2"	wordLine <u>220</u>	w/<10>
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# FIGURE 1B

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INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak, Andrew Wright

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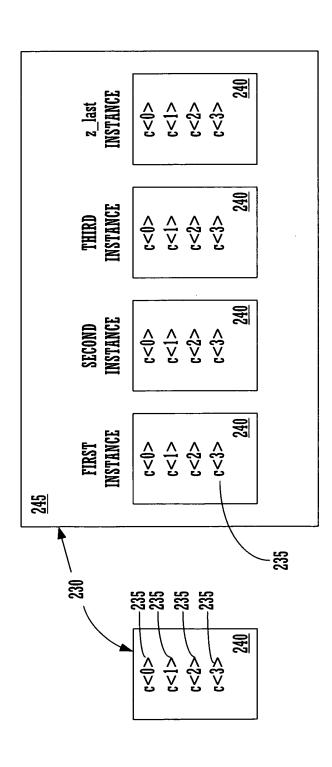


FIGURE 2A

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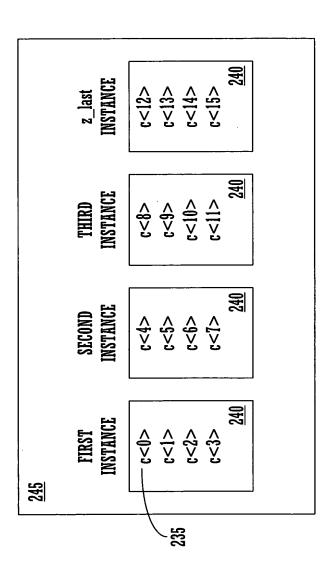


FIGURE 2B

TITLE: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA SUCTURE OF CONFIGURATION BITS FROM A SCHEMATIC

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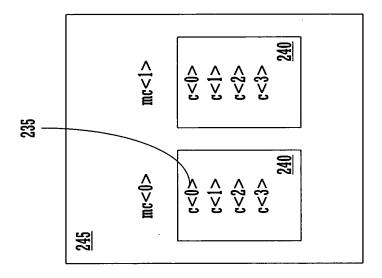
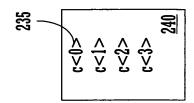
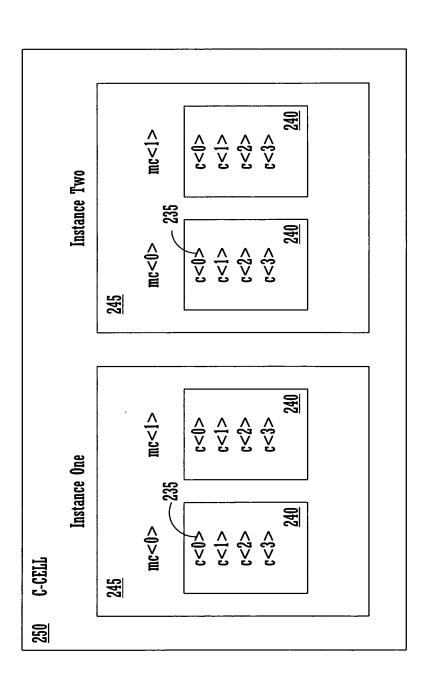


FIGURE 2C





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## FIGURE 2D

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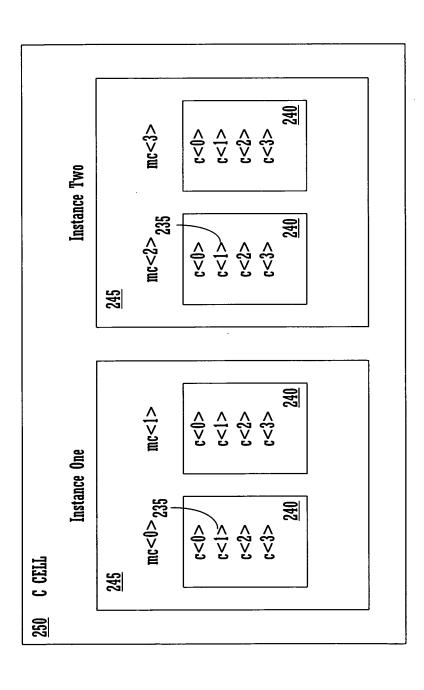
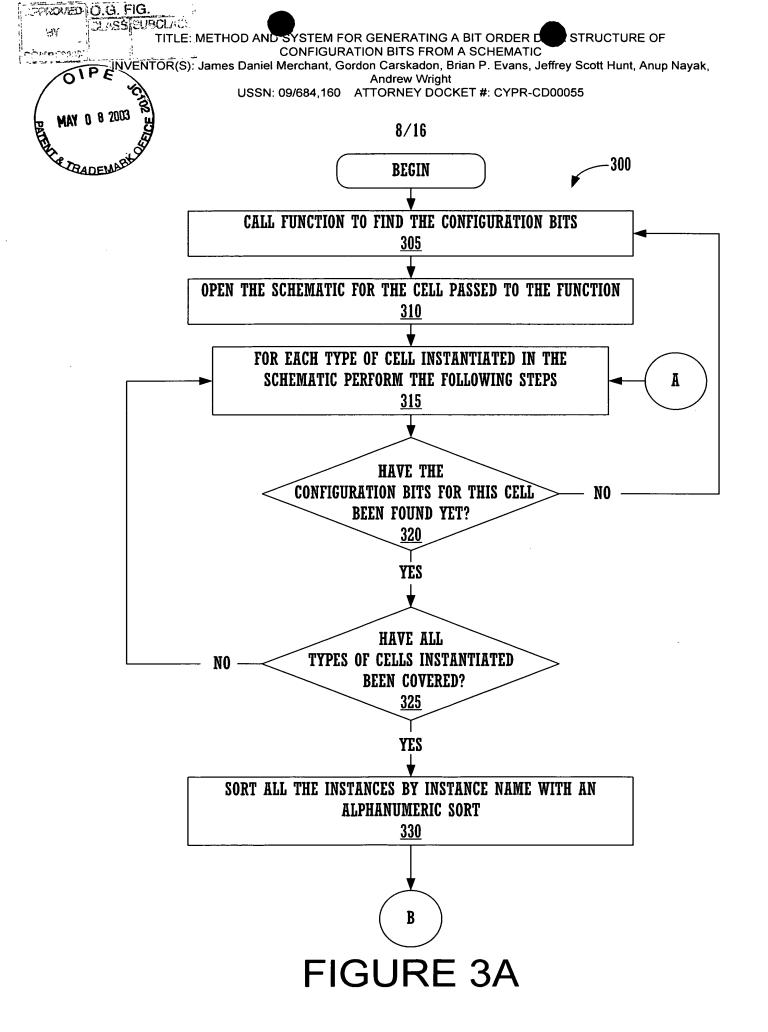
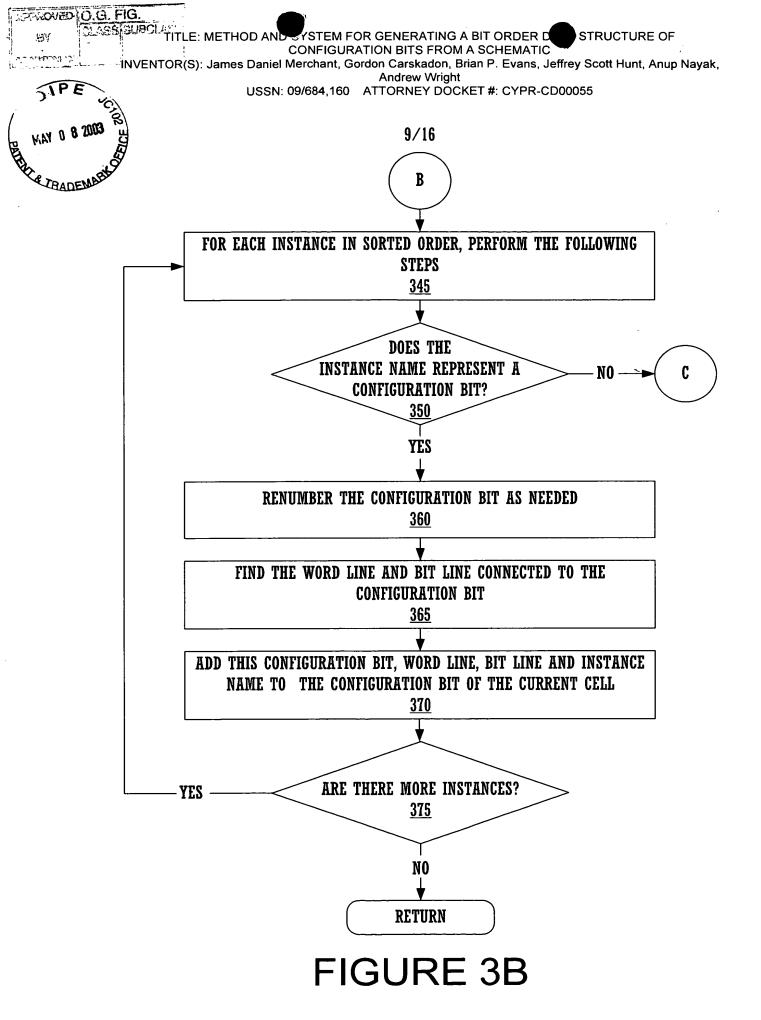
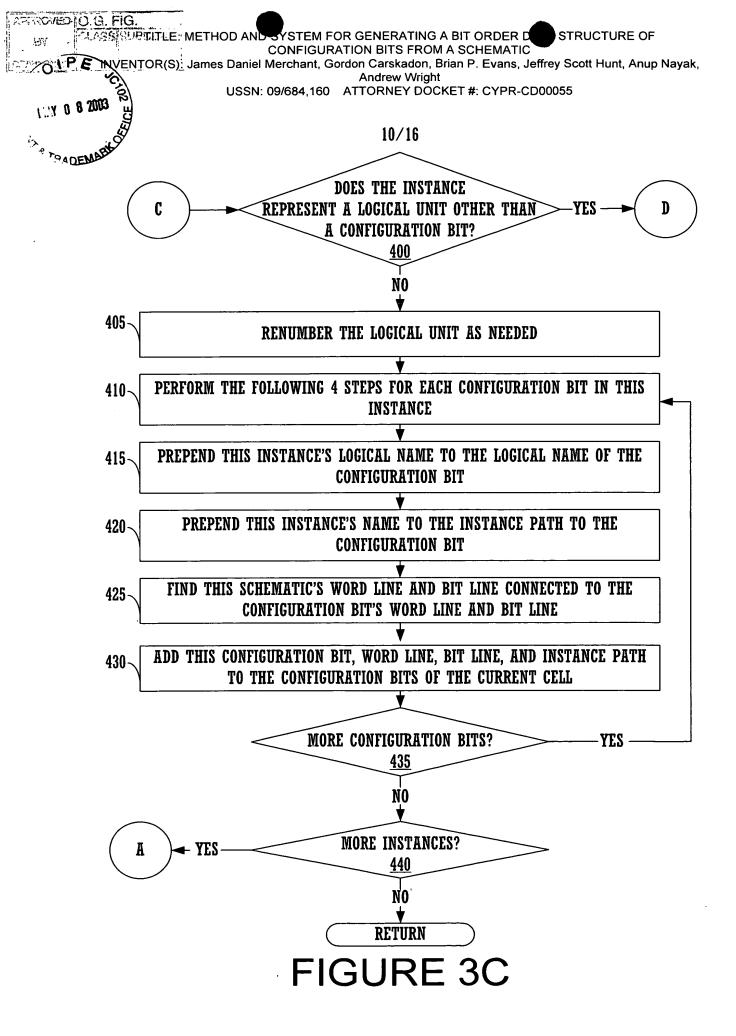
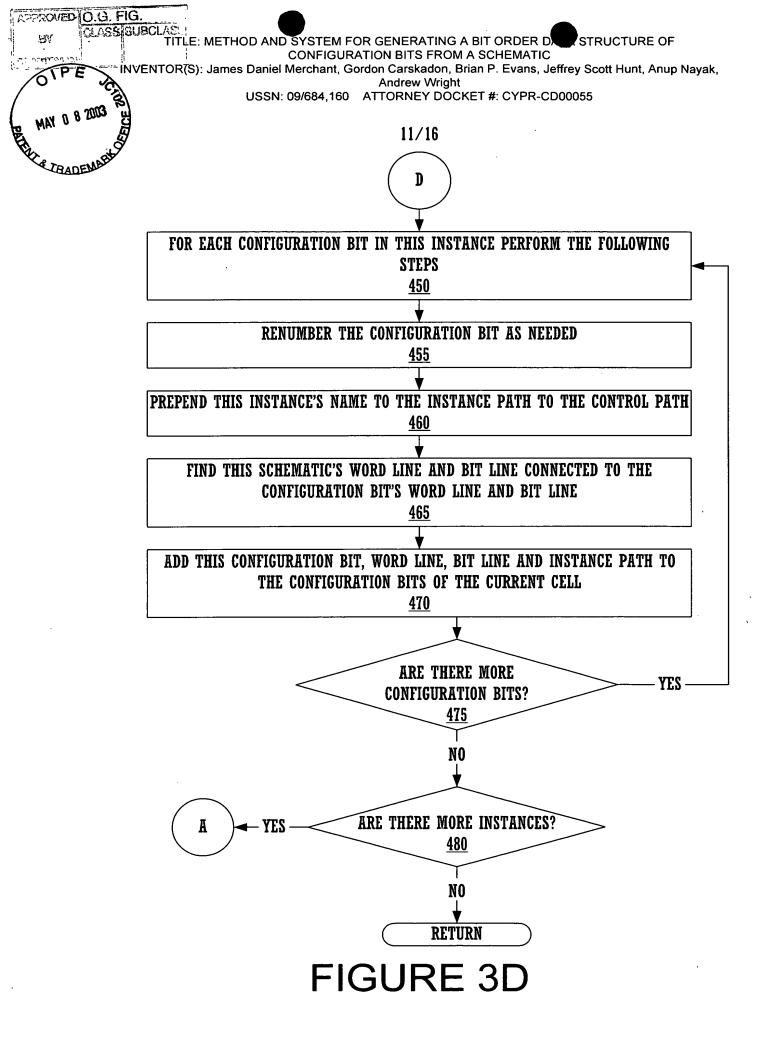


FIGURE 2E









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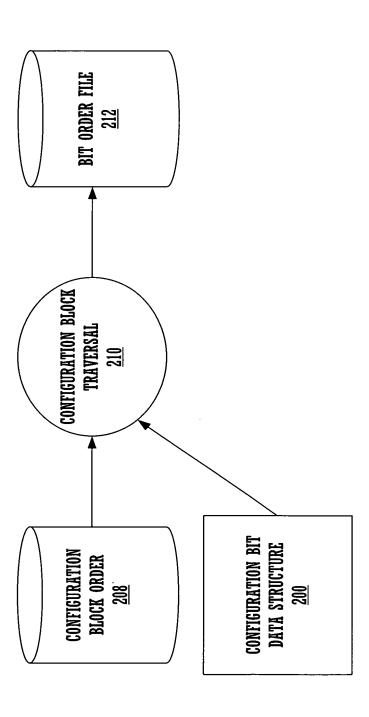


FIGURE 4A

TITLE: METHOD AND SYS FOR GENERATING A BIT ORDER DATA S CTURE OF CONFIGURATION BITS FROM A SCHEMATIC

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FIGURE 4B



```
begin c1 188 422
       1b < 0 > /mc < 0 > /c < 0 >
256
       1b < 0 > /mc < 0 > /c < 1 >
256
       1b<0>/mc<0>/c<2>
       spacer 8
       endWordLine 0
256
       1b<0>/mc<1>/c<0>
256
       1b<0>/mc<1>/c<1>
256
       1b<0>/mc<1>/c<2>
       spacer
       endWordLine 1
       cm<1>/crcfg<2>/c<0>
256 -
       cm<1>/crcfg<2>/c<1>
      cm<1>/crcfg<2>/c<2>
      cm<1>/crcfg<2>/c<3>
 258 end c1
 260 inst c1 c100
 260 inst c1 c101
 260 inst c1 c102
 260 inst c1
            c103
 260 inst cl c110
                                     212
```

## FIGURE 4C

INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak,
Andrew Wright
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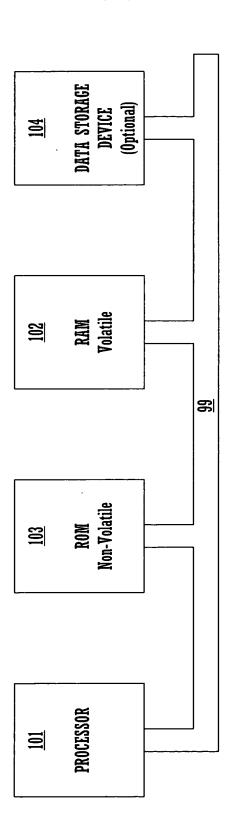


FIGURE 6

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